#9/B(AUG)
10/22/2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Ritsuko Iwasaki

Serial No.: 09/496,421 Group Art Unit: 2815

Filed: February 2, 2000 Examiner: Lee, E.

For: SEMICONDUCTOR DEVICE HAVING AN IMPROVED LAYOUT PATTERN OF PAIR TRANSISTORS

Honorable Assistant Commissioner of Patents
Washington, D.C. 20231
BOX AF

AMENDMENT UNDER 37 C.F.R. §1.116

Sir:

In response to the Office Action dated February 14, 2002, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Please amend the paragraph beginning at page 7, line 18 as follows:

– As shown for example in the non-limiting embodiment of Fig. 1, a dummy gate electrode may be arranged between a drain electrode of one transistor and a source electrode of an adjacent transistor on the element isolation region 50. Another dummy gate electrode may be arranged on the element isolation region 50 so that a source electrode of an adjacent transistor is sandwiched between the dummy gate electrode and the adjacent transistor. Also, a further dummy gate electrode may be arranged on the element isolation region 50 so that a drain electrode of an adjacent transistor is sandwiched between the dummy gate electrode and the adjacent transistor. The source electrode 15 is formed on the source diffusion region 5 to electrically connect with the source diffusion region 5 through contact 19 formed in an interlayer isolation layer between the source diffusion region 5 and the source electrode 15. The drain electrode 16 is formed on the drain diffusion region 6 to electrically connect with the drain diffusion region 6 through the contact 19 formed in the interlayer isolation layer. --

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